

Introduction

The PD64001 is a single-port Power over Ethernet PSE (Power Source Equipment) Manager. The PSE Manager allows for the detection of IEEE 802.3af-2003 and IEEE802.3at/D3.0 powered devices, ensuring safe power feeding and monitoring of Ethernet ports. With a minimum of external components, the PD64001 integrates in a one-port or two-port PoE-port switches and Midspans.

The PD64001 has several operating modes, allowing it to be tailored to the customer application, be it a Switch or a Midspan, IEEE802.af or IEEE802.3at/D3.0-compliant, with 1-event or 2-events classification, AC or DC disconnect and strict resistor detection or legacy detection capabilities. It operates in a total stand-alone mode, with no need for user intervention.

The PD64001 supports 2-events classification and operates at *Iport_max* currents of up to 720mA per port, making it fully compliant with the IEEE802.3at/D3.0

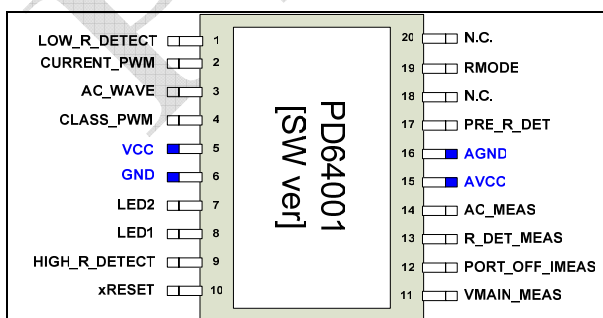
This datasheet includes a complete application note and provides detailed information and circuitry design guidelines for the implementation of a 1-port Power over Ethernet (PoE) system, based on Microsemi's™ 1-channel PoE device- the PD64001.

This document allows the designer to integrate PoE capabilities, as specified in the IEEE802.3af standard into an Ethernet switch, Midspan or a Router.

Applicable Documents

- ◆ IEEE802.3af-2003
- ◆ IEEE802.3at/D3.0

Pin Configuration



Features

- ◆ IEEE 802.3af-2003-compliant
- ◆ IEEE802.3at/D3.0 compliant
- ◆ Supports *Iport_max* of 720mA
- ◆ Programmable solution, can be updated as the IEEE802.3at standard evolves
- ◆ Accurate power measuring and extremely low power dissipation
- ◆ BOM and software tailored for specific application saving total solution cost
- ◆ Minimal power supply stress and EMI noises
- ◆ Legacy (pre-standard) PD's detection
- ◆ 1-port standalone PoE control
- ◆ 1-event and 2-event classification supported
- ◆ External FET and sense resistor
- ◆ AC and DC disconnect
- ◆ Detection of the disconnection method by assembled resistor
- ◆ Port On/Off Host interface
- ◆ Single operating voltage source
- ◆ Direct LED driving including IEEE802.3at indication
- ◆ SOIC-20 package
- ◆ RoHS compliant
- ◆ -40°C to +85°C operating ambient temperature

Ordering Information

| PART | TEMP. RANGE | PIN PACKAGE |
|---------|----------------|-------------|
| PD64001 | -40°C to +85°C | SOIC-20 |

Evaluation board ordering number - PD-IM-73001

Main Features Description

| Feature | Description |
|--|---|
| PD64001 features | |
| IEEE 802.3af-2003 Compliant | The PD64001 meets all IEEE-802.3af-2003 standard requirements such as: <ul style="list-style-type: none"> • Multi – point resistor detection • PD classification function • AC disconnect and DC disconnect function • Supports Back-off feature for Midspan implementation |
| IEEE802.3at/D3.0 Compliant | Including support for high power and 2-events classification. |
| Single DC Voltage Input | The PD64001 requires a single DC voltage source: 46V to 57V. No additional voltage sources (e.g. 3.3V/5V) are required for the PoE system's operation. |
| Wide temperature range: -40°C to +85°C | The PD64001 can operate over a wide temperature range: -40°C to +85°C. This wide temperature range allows the integration of the PD64001, into small unventilated boxes and operates in harsh environments. |
| Low thermal dissipation (1Ω sense resistor) | The PD64001 has a very low thermal dissipation. The Rsense in PD64001 applications is only 1Ω to keep the peripheral components in low temperatures as well. |
| External Power FET | External Mosfet, increasing the flexibility of the solution and allowing it to be tailored for the power needs of the customer. |
| H/W Disable Port | The PD64001 utilizes a dedicated pin, allowing an immediate disconnection of the PoE port. This disable-port pin can be controlled via the Host CPU. |
| Pre-Standard PD Detection | Enables detection and powering of pre-standard power devices (PDs). |
| Detection of Cisco Devices | Enables detection and powering of all Cisco devices including pre-standard terminals. |
| LED Support | Direct driving of the LED circuitry. It allows the designer to implement a simple LED circuit, indicating whether an IEEE802.3af or IEEE802.3at device is connected. |

Maximum Ratings

| | |
|---|---------------------------|
| V _{main} | -0.3 to 60 V |
| xRESETN input voltage..... | -0.5 to 5 V |
| Application circuitry DC current | 25 mA |
| ESD (Human Body Model)..... | -2V to 2kV ⁽¹⁾ |
| Lead temperature (soldering, 10 s)..... | 300 °C |

Notes:

⁽¹⁾ ESD testing is performed in accordance with the Human Body Model (CZap = 100 pF, RZap = 1500 Ω).

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

| PARAMETER | MIN. | NOM. | MAX. | UNIT |
|-----------------------------|------|------|------|------|
| Operating temperature | -40 | | +85 | °C |
| Storage temperature | -65 | | +150 | °C |
| Operational limitations (1) | 44 | 50 | 57 | V |

(1) In order to get higher power drive at the PSE output ports, it is recommended to use operating voltage source greater than 50v

Electrical Characteristics

DC Characteristics for Digital Inputs and Outputs

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | REMARKS |
|--------------------------|--|---------------------|-----------------------|------|----------------------|
| Pin Name | xRESET | | | | |
| Type | Schmitt Trigger CMOS input with internal pull-up | | | | |
| High level input voltage | V _{IH} | 0.9 V _{CC} | V _{CC} +0.5V | V | V _{CC} = 5V |
| Low level input voltage | V _{IL} | -0.5V | 0.2 V _{CC} | V | V _{CC} = 5V |
| Input high current | I _{IH} | | +1 | μA | |
| Input low current | I _{IL} | | +1 | μA | |
| Reset assertion time | T _{rst} | 2.5 | | μS | |
| Internal Pull-up value | R _{pu} | 30 | 60 | kΩ | |

Dynamic Characteristics

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|------|------|------|------|
| Automatic recovery from overload shutdown | TOVLREC value, measured from port shutdown (can be modified through control port) | | 8 | | s |
| Automatic recovery from no-load shutdown | TUDLREC value, measured from port shutdown (can be modified through control port) | | 1 | | s |

Thermal Data

Microsemi's PD64001 enables building very low power dissipating PoE devices. For a single port, the system worst case power dissipation can be calculated as follows.

| Application | Disconnection Method | I _{port_max} Current | R _{sense} (1Ω) | Diode | MOSFET | PoE Manager | Total |
|-------------|----------------------|-------------------------------|-------------------------|-------|---------------|-------------|-------|
| IEEE802.3af | DC | 350mA | 0.12W | - | 0.012W (0.1Ω) | 0.60W | 0.73W |
| IEEE802.3af | AC | 350mA | 0.12W | 0.53W | 0.012W (0.1Ω) | 0.60W | 1.26W |
| IEEE802.3at | DC | 720mA | 0.52W | - | 0.052W (0.1Ω) | 0.60W | 0.77W |
| IEEE802.3at | AC | 720mA | 0.52W | 1.08W | 0.052W (0.1Ω) | 0.60W | 1.85W |

Pin Functionality

| PIN | PIN NAME | PIN TYPE | PIN DESCRIPTION |
|-----|---------------|----------------|---|
| 1. | LOW_R_DETECT | Digital Output | Low level resistance detection command |
| 2. | CURRENT_PWM | Digital Output | Current limit set PWM output |
| 3. | AC_WAVE | Digital Output | AC disconnect output wave |
| 4. | CLASS_PWM | Digital Output | Class voltage set PWM output |
| 5. | VCC | VCC | 5V Digital VCC |
| 6. | GND | GND | Digital ground |
| 7. | LED2 | Digital Output | LED2 output command |
| 8. | LED1 | Digital Output | LED1 output command |
| 9. | HIGH_R_DETECT | Digital Output | High level resistance detection command |
| 10. | XRESET | Digital Input | Reset command from host |
| 11. | VMAIN_MEAS | Digital Output | Vmain measurement command |
| 12. | PORT_OFF_MEAS | Digital I/O | Port Off command/ current measurement input |
| 13. | R_DET_MEAS | Digital I/O | Port voltage measurement input |
| 14. | AC_MEAS | Digital I/O | AC disconnect measurement input |
| 15. | AVCC | VCC | 5V Analog VCC |
| 16. | AGND | GND | Analog ground |
| 17. | PRE_DET | Digital Output | Pre detection command |
| 18. | RESERVED1 | Digital I/O | Reserved |
| 19. | RMODE | Digital Input | POE manager mode setup |
| 20. | RESERVED2 | Digital I/O | Reserved |

R Mode Pin

This pin is connected to a resistor voltage divider. It allows the user to choose a combination of three features, as specified in the following table:

| R_mode Voltage | ALT A | ALT B | CA P | AT | R26 (Ω)* |
|----------------|-------|-------|------|----|----------|
| 0.313 – 0.62 V | X | | | | 1.02K |
| 0.94 – 1.25 V | | X | | | 2.8K |
| 1.563 – 1.87 V | X | | X | | 5.23K |
| 2.19 – 2.5 V | | X | X | | 8.87K |
| 2.82 – 3.1 V | X | | | X | 14.7K |
| 3.44 – 3.75 V | | X | | X | 25.5K |
| 4.06 – 4.375 V | X | | X | X | 54.9K |
| 4.68 – 5 V | | X | X | X | No |

* R26 Pull-down's value depends on the actual mode, while for all of the modes, R25 Pull-up's value is 10Kohm.

The ALT A / ALT B option is selecting between a PSE alternative A or PSE alternative B. For implementing a Midspan PSE use ALT B. The AT option is IEEE802.3at- Compliant in accordance with the IEEE802.3at/D3.0. The CAP option is pre standard Capacitor detection mode.

General Application Description

The circuit includes the following major interfaces with the Host board:

Control

A Reset control signal driven by the switch circuitry is used to reset the PoE circuit. This signal should be optically coupled by the Host in order to maintain the requirements for the 1500 Vrms isolation.

Power Supply Mains

The PoE system operates over a range of 44V to 57V.

This power must be isolated from the switch supply and chassis by 1500 Vrms.

Grounds

There are several grounds used in the system: chassis, digital and analog. The chassis ground is connected to the switch's chassis ground.

This ground plane should be 1500Vrms isolated from the PoE circuitry as well as the power supply for the PoE circuitry. The digital and analog grounds are electrically the same ground. However, in order to reduce noise coupling, the grounds are physically separated and connected only at a single point.

5V Regulator

A single port application includes a 5V regulator (Vcc) fed by the Vmain through D15, D16 zener diodes and provides up to 25mA which is used to power the CPU and external components in the PoE domain.

The D15 and D16 should be selected for the application main voltage as follows:

For $44V \leq V_{main} < 50V$ use 16V zener diode.

For $50V \leq V_{main} \leq 57V$ use 20V zener diode.

If an adequate 5V power source is available, the 5V regulation circuitry can be removed and the zener diodes may be replaced by lower current (5mA) zener diodes but with same voltage requirements.

Detailed Application Description

(See Figure 1)

The PD64001 performs a multitude of internal operations and PoE functions, requiring a bare minimum of external components.

The device is based on Atmel's ATtiny461 MCU.

Each PD64001 device handles one port. Figure 1 shows the device with its related components for a 1-port configuration.

Mode Configuration - set by the resistor divider (R25/R26) tied in to the RMODE line. The values are fixed for each mode of operation and described in the "R Mode pin" section in this document.

Line Detection Circuitry – when performing a line detection procedure, the PoE device utilizes certain voltage levels over the output port. These levels are produced by switched resistor dividers and sensed by the PD64001 in order to confirm a valid PD connection.

Current Loop Circuitry – the current is controlled by Q3 MOSFET. The PD64001 supplies PWM signal via pin#2 with a constant duty cycle (depending on the R mode configuration). This PWM signal is filtered and utilized as the current limit circuitry voltage reference.

Sense Resistors – for each powered port, two 2-Ohm 2010 (1%) resistors connected in parallel (1-Ohm equivalent) are used in series with the output. In cases where the ambient temperature drops below 70°C, or the product does not have to meet 802.3at power, a single 1-Ohm 2010 (1%) resistor is adequate.

Classification Circuitry – After a port is investigated, the PD should be classified by a classification current signature.

Two voltage levels are set over the port, derived from a reference voltage filtered from PD64001 pin#4 (PWM signal) and sent to an operational amplifier which controls Q3 MOSFET.

Output port - The load resistance of the PD attached to the port is presented in parallel with R30.

The resulting voltage developed across both resistances is monitored to establish the 802.3af/at compatibility.

LED indication - The 1 port application may use the PD64001 LED1 and LED2 pins for system status indications as follows.

| PD operating Status | LED1 | LED2 |
|----------------------|--------------|--------------|
| IEEE802.3af – ON | ON | OFF |
| IEEE802.3at – ON | ON | ON |
| IEEE802.3af - OVL/SC | Blink at 1Hz | OFF |
| IEEE802.3at - OVL/SC | Blink at 1Hz | Blink at 1Hz |
| Vmain out of range | Blink at 1Hz | OFF |

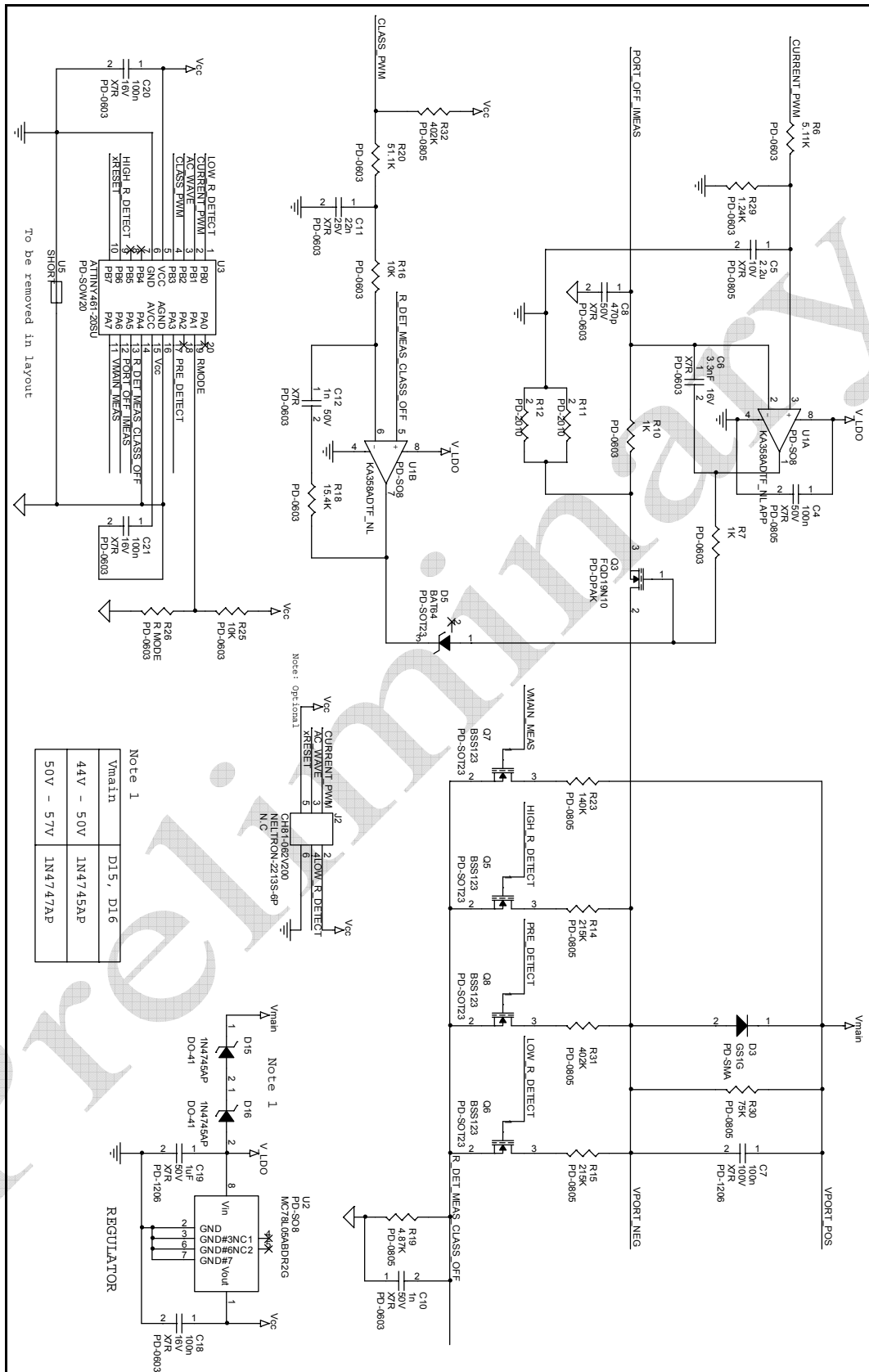


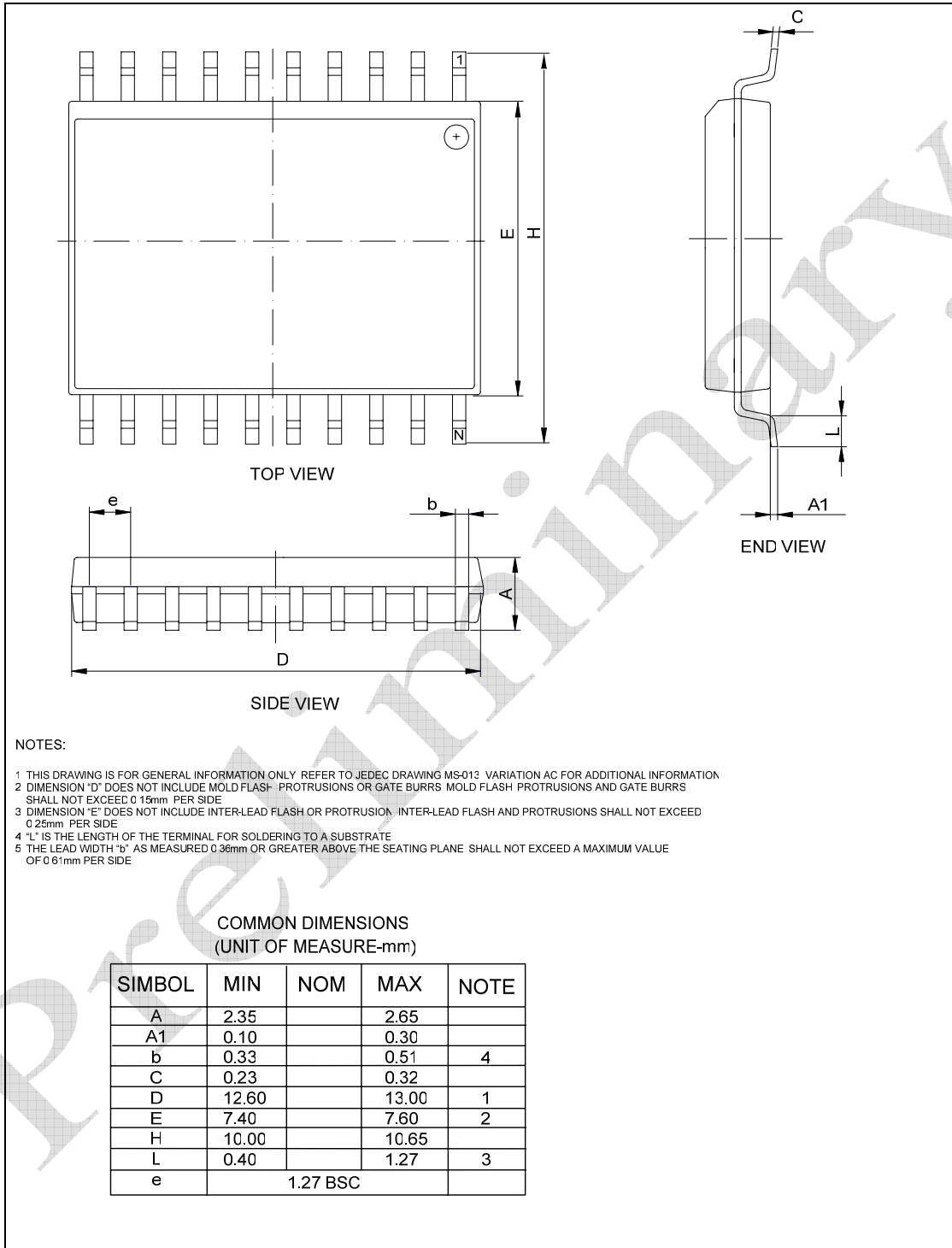
Figure 1: One Port Chipset Schematic Diagram

Bill of Materials for a PoE System

| Block | QTY | Reference | Description | PCB Footprint | Manufacturer | Manufacturer's Part Number |
|--------------------------|-----|----------------|---|---------------|--------------|----------------------------|
| 1 port Chipset Circuitry | 1 | C4 | CAP CRM 100nF 50V 10% X7R 0805 SMT | PD-0805 | Samsung | CL21B104KBAC |
| | 1 | C5 | CAP CRM 2.2uF 10V 10% X7R 0805 SMT | PD-0805 | Samsung | CL21B225KPFNNNC |
| | 1 | C6 | CAP CRM 3.3nF 16V 10% X7R 0603 SMT | PD-0603 | TDK | C1608X7R1C332K |
| | 1 | C7 | CAP CRM 100nF 100V 10% X7R 1206 SMT | PD-1206 | Samsung | CL31B104KCFNNNE |
| | 1 | C8 | CAP CRM 470pF 50V 10% X7R 0603 SMT | PD-0603 | EPCOS | B37931-K5471-K60 |
| | 2 | C10, C12 | CAP CRM 1nF 50V 10% X7R 0603 SMT | PD-0603 | EPCOS | B37931-K5102-K60 |
| | 1 | C11 | CAP CRM 22nF 25V 10% X7R 0603 SMT | PD-0603 | Rohm | MCH185CN223KK |
| | 3 | C18, C20, C21 | CAP CRM 100nF 16V 10% X7R 0603 SMT | PD-0603 | EPCOS | B37931K9104K60 |
| | 1 | C19 | CAP CRM 1uF 50V 10% X7R 1206 SMT | PD-1206 | TDK | C3216X7R1H105K |
| | 1 | D3 | DIO REC 400V 1A SMA SMT | PD-SMA | Pan Jit | GS1G |
| | 1 | D5 | DIO SCHOT 30V 200mA SNGL SOT23 SMT | PD-SOT23 | Infineon | BAT64 |
| | 2 | D15, D16 | DIODE 16V 1W 5% D041 Insert | DO-41 | Microsemi | 1N4745AP |
| | 1 | Q3 | FET NCH 100V 13A 0.12R DPAK SMT | PD-DPAK | Fairchild | FQD19N10 |
| | 4 | Q5, Q6, Q7, Q8 | FET NCH 100V 0.15A 6R Logic Level SOT23 | PD-SOT23 | Infineon | BSS123 |
| | 1 | R6 | RES 5.11K 62.5mW 1% 0603 SMT MTL FLM | PD-0603 | Samsung | RC1608F5111CS |
| | 1 | R7 | RES 1K 62.5mW 1% 0603 SMT MTL FLM | PD-0603 | Rohm | MCR03EZHEF1001 |
| | 1 | R10 | RES 1K 62.5mW 1% 0603 SMT MTL FLM | PD-0603 | Samsung | RC1608F1001CS |
| | 2 | R11, R12 | RES 2R 0.75W 1% 2010 SMT TCK FLM | PD-2010 | KOA | RK73H2HTTE2R00F |
| | 2 | R14, R15 | RES 215K 0.125W 0.5% 0805 | PD-0805 | Yageo | RT0805DRD07215K |
| | 2 | R16, R25 | RES 10K 62.5mW 1% 0603 SMT MTL FLM | PD-0603 | Rohm | MCR03EZHEFX1002 |
| | 1 | R18 | RES 15.4K 62.5mW 1% 0603 SMT TCK FLM | PD-0603 | Samsung | RC1608F1542CS |
| | 1 | R19 | RES 4.87K 125mW 1% 0805 SMT TCK FLM | PD-0805 | XXX | XXX |
| | 1 | R20 | RES 51.1K 62.5mW 1% 0603 SMT MTL FLM | PD-0603 | Samsung | RC1608F5112CS |
| | 1 | R23 | RES TCK FLM 140K 1% 125mW 0805 SMT | PD-0805 | Samsung | RC2012F1403CS |
| | 1 | R26 | R mode | PD-0603 | | |
| | 1 | R29 | RES 1.24K 62.5mW 1% 0603 SMT TCK FLM | PD-0603 | ASJ | CR16-1241FL |
| | 1 | R30 | RES 75K 125mW 1% 0805 SMT TCK FLM | PD-0805 | Rohm | MCR10EZHEF7502 |
| | 2 | R31, R32 | RES 402K 125mW 1% 0805 SMT MTL FLM | PD-0805 | Yageo | RC0805FRF07402K |
| | 1 | U1 | OP AMP DUAL 32V LOW OFFSET SO8 | PD-SO8 | Fairchild | KA358ADTF_NL |
| | 1 | U2 | IC VOLT REG 5V 0.1A 4% SO8 SMT | PD-SO8 | ON Semi | MC78L05ABDR2G |
| | 1 | U3 | Microcontroller 2K 8-bit SOIC-20 SMT | PD-SOW20 | Microsemi | PD64001 |

Package Information

Microsemi's PD64001 is housed in a 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC).



Revision History

| Revision Level / Date | Para. Affected | Description |
|-----------------------|-------------------------------------|---|
| 0.1 / 26 November, 07 | - | Initial Release |
| 0.2 / 25 December 07 | Introduction | Introduction, Features and ordering information added |
| 0.3 / 28 March 08 | schematic diagram | Schematic diagram and BOM has been updated |
| 0.4 / 04 May 08 | Whole document schematic diagram | General updates Schematic diagram and BOM had been updated |

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